CLAIMS

What is claimed is:

1. A method of performing multiple operations on a memory device, comprising:

dividing the memory device into k partitions, wherein k is an integer greater than or equal to two;

performing code operations from m code partitions out of k total partitions, wherein m is an integer greater than or equal to one; and

performing data operations from n data partitions out of k total partitions through low level functions accessed from the code partitions, wherein n is an integer greater than or equal to one.

2. The method of claim 1, wherein the data partitions and the code partitions do not overlap each other in the memory device.

3. The method of claim 1, wherein the m code partitions and the n data partitions equal the k total partitions.

4. The method of claim 3, wherein each of the m code partitions are equal in size to each of the n data partitions.

5. The method of claim 3, wherein the m code partitions and the n data partitions are fixed in memory space.

6. The method of claim 1, wherein the memory device is a flash memory.

7. The method of claim 6, wherein the flash memory is a flash electrically erasable read only memory (EEPROM) array.

8. An apparatus comprising:

means for partitioning a memory device to enable multiple operations to be performed on a memory device at the same time; and

means for tracking operations performed on the device to restore interrupted tasks.

9. The apparatus of claim 8, further comprising a means for saving a preempted operation before entering an interrupt routine.

10. The apparatus of claim 8, further comprising a means for restoring a preempted task following an interrupt routine.

11. A memory array, comprising:

a plurality of partitions;

a status mode to provide partition status from the memory device;

a read mode to read code and data from the memory device; and

a write mode to write data to the memory device.

12. The memory array of claim 11, wherein the code is programmed into the memory array.

13. The memory array of claim 11, wherein the write mode is also capable of performing erase operations on data stored in the memory array.

14. The memory array of claim 11, wherein the memory array is a flash memory array.

15. A method of handling a preemption within a flash memory device, comprising the steps of:

saving the preempted state;

reading the current state from the flash memory device;

determining whether the flash memory device is busy;

setting the memory device to a preempting state, wherein the preempting state is determined by the preempting command;

issuing a preempting command;

executing the preempting command; and

restoring the preempted state.

16. The method of claim 15, further comprising the step of suspending a preempted task if the flash memory device is busy prior to issuing a preempting command.

17. The method of claim 15, further comprising the step of disabling interrupts prior to issuing the preempting command if the preempting command is a write, erase, or copy.

18. The method of claim 17, further comprising the step of enabling interrupts following the completion of the preempting command.

19. An apparatus, comprising;

a memory device with k partitions, wherein k is an integer greater than or equal to two;

low level functions to access the memory device; and

a flag to indicate when a suspend operation has occurred.

20. The apparatus of claim 19, wherein the memory device comprises:

m code partitions, wherein m is an integer greater than or equal to one; and

n data partitions, wherein n is an integer greater than or equal to one.

21. The apparatus of claim 19, wherein the memory device is a flash memory.

22. A method of performing a preempting copy operation, comprising the steps of:

placing the current state in read mode;

issuing the read command to access data to be copied;

retrieving the data to be copied;

placing the current state in status mode;

disabling interrupts;

unlocking a memory block to be written;

performing a write setup; and

writing the data to memory.

23. The method of claim 22 further comprising the step of enabling interrupts following the completion of the preempting copy operation.

24. The method of claim 22, wherein the memory block is a flash memory block.